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am335x pru icss reference guide rev a

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Introduction

Embedded developers who work with Texas /Instruments' AM335x family of processors often rely on the Programmable Real Time Units (PRUs) and the Integrated Communications Subsystem (ICSS) to achieve deterministic, high throughput I/O. The **am335x pru icss reference guide rev /a** is the definitive source of information for these peripherals, offering a deep dive into hardware registers, memory maps, and programming paradigms. Whether you're building a motor controller, a sensor network, or a high speed data acquisition system, understanding this reference guide is essential for unlocking the full potential of the AM335x platform.

What Is the AM335x Family?

The AM335x series is a line of ARM Cortex A8 processors designed for industrial and automotive applications. Each SoC integrates a single core CPU, a rich set of peripherals, and a powerful PRU/ICSS subsystem. The processors run at frequencies up to 800 MHz and feature a 32 bit memory bus, making them ideal for real time control tasks.

Key attributes include:

- ARM Cortex A8 core with NEON SIMD extensions
- 1 /MB L2 cache
- Integrated DDR2/DDR3/LPDDR2 memory controller
- USB, SATA, PCIe, and Ethernet interfaces
- Embedded PRU/ICSS for deterministic I/O

Understanding PRU and ICSS

The PRU subsystem consists of two microcontrollers (PRU0 and PRU1) that operate at 200 MHz, independent of the main CPU. They are ideal for low latency tasks such as motor control, digital signal processing, or custom communication protocols.

The ICSS (Integrated Communications Subsystem) extends the PRU functionality by adding a dual port Ethernet MAC, DMA engines, and a set of programmable I/O pins. In revision /A, the ICSS provides:

1. Two independent PRU cores
2. Two DMA channels per PRU
3. Ethernet MAC with 10/100 /Mbps support
4. Programmable I/O (PINS) for custom signaling
5. Clock and reset control registers

Why Revision /A Matters

Revision A of the reference guide introduces critical updates that reflect hardware revisions in newer AM335x devices. These changes include:

- New register definitions for the PRU Control and Status registers

- Updated memory map for the ICSS peripheral space
- Additional notes on power down sequencing
- Clarifications on the interaction between PRU interrupts and the main CPU

Using the most recent revision ensures compatibility with the latest board revisions and avoids subtle bugs that may arise from outdated documentation.

Hardware Overview of the PRU/ICSS Block

Memory Map

The PRU/ICSS occupies a contiguous region in the AM335x memory space. The reference guide provides a detailed table that maps each register to a specific offset. For example:

- 0x44E0_8000 – PRU0 Control Register
- 0x44E0_8004 – PRU0 Status Register
- 0x44E0_8010 – PRU0 Data RAM
- 0x44E0_8020 – PRU0 Instruction RAM
- 0x44E0_8030 – PRU0 DMA Channel 0 Register
- 0x44E0_8040 – PRU0 DMA Channel 1 Register
- 0x44E0_8050 – PRU0 DMA Channel 2 Register
- 0x44E0_8060 – PRU0 DMA Channel 3 Register

Each block is 64 bytes wide, and the entire PRU/ICSS space spans 0x2000 bytes. This layout is crucial for low level programming, especially when setting up DMA transfers or configuring the Ethernet MAC.

Clock and Reset Control

The PRU subsystem is clocked by the *PRU_CLK* source, which can be gated or divided to reduce power consumption. The reference guide specifies the register **PRU_CLKCTRL** at offset 0x44E0_80C0, which controls:

- Clock enable/disable
- Clock division factor
- Reset status and control

Properly managing these registers is essential for reliable operation, especially in power critical applications.

Programming the PRU

Assembly vs. C

PRU code can be written in assembly or C. TI's *PRUware*compiler provides a C compiler that translates code into PRU instruction sets. The reference guide lists the instruction set architecture (ISA) details, including supported opcodes, operand sizes, and addressing modes.

Typical steps for PRU development include:

1. Write the code in .c or .S format.
2. Compile with pru-gcc or pru-ld.
3. Load the binary into PRU instruction RAM using the prussdrv library.
4. Configure the PRU's data RAM for inter processor communication.
5. Set up interrupts or DMA if required.

Data RAM and Shared Memory

The PRU features 8 /KB of data RAM per core, accessible via **PRU0_DMEM** and **PRU1_DMEM**. The reference guide describes the memory layout, alignment constraints, and how to map shared memory between the PRU and the ARM CPU. A common pattern is to use a *mailbox* in data RAM for command/response exchanges.

Interrupts and Event Handling

PRU interrupts are routed through the **PRU_EVTOUT** and **PRU_EVTOUT_CFG** registers. The guide explains how to configure event sources, such as external GPIO pins or internal timers, and how to handle them in the PRU code. For example, to trigger an event on a rising edge of a GPIO pin, you would set the corresponding bit in **PRU_EVTOUT_CFG** and enable the pin in the **GPIO_OE** register.

DMA Configuration

The PRU's DMA engines are powerful tools for high throughput data movement without CPU intervention. The reference guide lists the DMA channel registers (e.g., **PRU0_DMA_CH0_CFG**) and explains the fields:

- Source and destination addresses
- Transfer length
- Transfer mode (cyclic, single, burst)
- Interrupt enable

Typical use cases include streaming sensor data to DDR memory or feeding an Ethernet MAC buffer.

Using the ICSS Ethernet MAC

PHY Initialization

The ICSS Ethernet MAC requires a PHY to be initialized. The reference guide outlines the standard MDIO interface for register access and lists the PHY's capabilities. A typical initialization sequence involves:

1. Resetting the PHY via MDIO register 0x0.
2. Reading the PHY status register 0x1 to verify link.
3. Configuring auto negotiation settings.

Transmit and Receive Buffers

Packets are transferred between the PRU and the MAC via DMA descriptors. The guide provides the descriptor format, including fields such as **DESC_STATUS**, **DESC_LENGTH**, and **DESC_ADDR**. Proper alignment (usually 16 byte) is essential for optimal performance.

Interrupt Handling

When a packet is received or transmitted, the MAC raises an interrupt to the PRU. The reference guide details the **PRU_ICSS_IRQ** register and how to mask or unmask specific events. The PRU code must clear the interrupt flag after processing to avoid spurious interrupts.

Development Environment Setup

Tools Required

- TI Code Composer Studio (CCS) – IDE for ARM and PRU development
- TI PRUware – compiler and linker toolchain
- TI PRUSS SDK – libraries and drivers for PRU interaction
- Linux or Windows host with USB to UART bridge for board communication

Board Configuration

When working with evaluation boards (e.g., BeagleBone Black, AM335x Starter Kit), the bootloader must be configured to load the PRU firmware. The reference guide includes a boot script example that copies the PRU binary from the root filesystem into the PRU's instruction RAM during boot.

Debugging Techniques

Debugging PRU code can be challenging. The guide recommends the following:

- Use the prussdrv library's PRUSS_DRV_DEBUG flag.
- Insert __asm__ volatile("NOP"); instructions to create breakpoints.
- Leverage the CCS debugger's "Remote Target" mode to attach to the PRU core.
- Monitor DMA status registers for transfer completion.

Common Use Cases

Motor Control

PRUs excel at implementing pulse width modulation (PWM) and closed loop control algorithms. Using the PRU's I/O pins, developers can generate high frequency PWM signals with minimal jitter, while the ARM CPU handles higher level logic.

High Speed Data Acquisition

By configuring the PRU DMA channels to stream data directly into DDR memory, a system can capture sensor data at rates exceeding several megabytes per second without burdening the CPU.

Custom Communication Protocols

Some industrial protocols (e.g., EtherCAT, CAN FD) require deterministic timing. PRUs can implement these protocols in software, providing flexibility while meeting strict timing constraints.

Frequently Asked Questions

1. What is the difference between PRU0 and PRU1? PRU0 and PRU1 are identical cores but operate independently. PRU0 is often used for time critical tasks, while PRU1 can handle secondary processing or act as a DMA controller.
2. Can I run Linux on the AM335x while using PRUs? Yes. The PRUs run in parallel with the ARM Cortex A8 core and can be used alongside a Linux kernel.
3. How do I handle power management for the PRU? The reference guide recommends gating the PRU clock via PRU_CLKCTRL during idle periods and using the PRU_PWR registers to control power state.
4. Is the Ethernet MAC limited to 100 /Mbps? The ICSS Ethernet MAC in AM335x supports 10/100 /Mbps. For Gigabit Ethernet, a separate Gigabit PHY and MAC are required.

Conclusion

The **am335x pru icss reference guide rev /a** is an indispensable resource for developers who need to harness the deterministic power of PRUs and the versatility of the ICSS on the AM335x platform. By mastering the hardware registers, memory maps, and programming models outlined in the guide, engineers can create robust, high performance embedded systems that meet stringent real time requirements. Whether you're building a precision motor controller, a high speed data logger, or a custom communication stack, the reference guide provides the clarity and depth needed to bring your project from concept to production.

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