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altera high definition multimedia interface ip core user guide

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Altera High Definition Multimedia Interface (HDMI) IP Core User Guide

Embedded multimedia is rapidly becoming the backbone of modern consumer electronics, automotive infotainment, medical imaging, and industrial automation. When designing an FPGA based system that must transmit high definition video and audio over HDMI, the **Altera HDMI IP core** (now part of Intel's FPGA IP library) offers a turnkey solution that abstracts the complex HDMI protocol stack while delivering low latency, high throughput performance. This comprehensive user guide walks you through every step—from understanding the core's architecture to deploying a fully functional HDMI transmitter or receiver on your target board. Whether you're a seasoned FPGA engineer or a newcomer to video interfaces, this guide will help you harness the power of the Altera HDMI IP core with confidence and efficiency.

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1. Overview of the HDMI IP Core

The Altera HDMI IP core encapsulates the entire HDMI 1.4/2.0 protocol stack—including TMDS data encoding, clock recovery, packet framing, and ancillary data handling—into a reusable, synthesis ready module. By integrating this core into your Quartus Prime project, you eliminate the need to implement low level TMDS logic manually, which is notoriously error prone and time consuming.

At its heart, the core consists of two primary blocks: the **HDMI Transmitter** and the **HDMI Receiver**. Each block is further subdivided into *Video*, *Audio*, and *Control* sub modules, allowing designers to enable or disable features as

needed. The IP core supports a wide range of video resolutions (up to 4096×2160 at 60 Hz) and audio formats (PCM, LPCM, and compressed streams), making it suitable for both consumer displays and professional broadcast equipment.

2. Key Features and Capabilities

- Full HDMI 1.4/2.0 Compliance: Supports all required packet types, including CEC, HDCP, and EDID.
- High Speed TMDS Encoding: Optimized for 3 /Gbps per data lane, ensuring robust signal integrity.
- Flexible Clock Domain Support: Works with both single clock and multi clock designs, leveraging PLLs or DCMs for clock generation.
- Integrated Audio Processing: Handles PCM, LPCM, and compressed audio streams up to 7.1 channels.
- Variable Refresh Rate (VRR) and HDR: Configurable to support HDR10, Dolby Vision, and dynamic range adjustments.
- HDCP 2.2 Encryption: Optional hardware acceleration for secure content transmission.
- Low Latency Pipeline: End to end latency as low as 20 /ns for 1080p video.
- Extensible Packet Handling: Custom packet insertion and extraction for vendor specific data.
- Comprehensive Debug Interface: Built in AXI Lite control and status registers for real time monitoring.
- IP Core Versioning: Multiple releases (v1.0, v1.1, v2.0) with backward compatibility and bug fixes.

3. System Requirements and Supported Platforms

The HDMI IP core is designed to run on Intel's Cyclone V, Arria V, Cyclone V GX, Arria 10, and Stratix 10 families. It requires the following software stack:

- Quartus Prime 17.0 or later (Standard/Pro/Ultimate)
- Intel FPGA SDK for OpenCL (optional, for OpenCL based designs)
- Intel Quartus Prime Design Suite (including IP Catalog and IP Integrator)
- Intel FPGA Board Support Packages (BSPs) for target development boards
- Intel Quartus Prime Simulation (ModelSim/Verilog Sim) for functional verification

Hardware prerequisites include a board with a 3 lane TMDS interface, a 75 :• differential pair routing, and a suitable clock source (typically a 148.5 MHz reference for 1080p). For HDCP enabled designs, a secure key storage module is required.

4. Licensing and IP Versioning

Intel offers the HDMI IP core under a **Commercial License** for commercial projects and an **Academic License**for educational use. Each license grants access to the IP catalog, documentation, and support. The core is versioned as follows:

1. v1.0 – Initial release supporting HDMI 1.4.
2. v1.1 – Added support for 4K resolution and minor bug fixes.
3. v2.0 – Full HDMI 2.0 compliance, HDR10 support, and HDCP 2.2 encryption.

When upgrading, ensure that the target FPGA family remains compatible. The IP catalog will automatically flag any unsupported configurations.

5. Installation and Setup in Quartus Prime

Follow these steps to add the HDMI IP core to your Quartus project:

1. Open Quartus Prime and create a new project or open an existing one.
2. Navigate to the IP Catalog by selecting Tools > IP Catalog.
3. Search for “HDMI”. The catalog will display the HDMI Transmitter and Receiver cores.
4. Double click the desired core (e.g., “HDMI Transmitter”) to launch the IP Configuration wizard.
5. Follow the wizard prompts to select your target device family, clock sources, and desired features.
6. Generate the IP. Quartus will create a new IP instance in your project directory.
7. Add the generated IP to your design hierarchy by dragging it from the IP Catalog into the Design Files tree.
8. to verify that the IP is integrated correctly.

Tip: Use the **IP Catalog Manager**to keep track of multiple HDMI instances, especially when designing systems with both transmitter and receiver blocks.

6. Design Flow: From IP Integration to Bitstream Generation

Once the HDMI IP core is instantiated, you’ll need to follow a structured design flow to ensure a successful synthesis, implementation, and verification:

1. Design Entry: Create your top level HDL module and instantiate the HDMI IP. Connect the video_in, audio_in, and control_in ports to your source modules.
2. Clock Management: Use the PLL or MMCM IP to generate the required TMDS clock (typically 148.5 /MHz) and any auxiliary clocks.
3. Signal Routing: Assign the TMDS differential pairs to the correct physical pins using the Pin Planner. Ensure that the routing constraints meet the required 75 /:’ F–f`erential impedance.
4. Synthesis: Run the synthesis process. Watch for any timing violations or resource over utilization warnings.
5. Implementation: Perform place and route, paying attention to the timing reports for the TMDS data lanes.
6. Simulation: Use the built in simulation models (VHDL/Verilog) provided by the HDMI IP core to verify functional correctness. Simulate both video and audio streams.
7. Bitstream Generation: Generate the configuration file (.sof/.pof) and load it onto the target board.
8. Hardware Verification: Connect the board to a monitor or capture device. Verify that video and audio playback is correct, and that EDID negotiation and HDCP authentication (if enabled) succeed.

7. Core Configuration Parameters

The HDMI IP core exposes a rich set of configuration parameters that can be tuned to match your system’s requirements. Below is a non exhaustive list of the most critical settings:

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